

What is claimed is:

- 1 1. A package for an integrated circuit, comprising:
 - 2 a plurality of layers sealably connectable to each other to form a package having a
 - 3 cavity sized and shaped to receive the integrated circuit, each layer being formed of a
 - 4 respective material, each respective material being suitable for use as a printed circuit
 - 5 board substrate,
 - 6 at least one of the plurality of layers being a substrate having contacts that are
 - 7 connectable to electrical contacts of the integrated circuit, and
 - 8 a bottom one of the layers having a plurality of ball attach pads, electrically
 - 9 connected to the contacts of the substrate.
- 1 2. The package of claim 1, wherein one of the layers is a superstrate above the
- 2 substrate, the superstrate having a sufficiently high dielectric constant to provide isolation
- 3 between a plurality of signal traces on the substrate.
- 1 3. The package of claim 2, wherein the superstrate is formed of the same material as
- 2 the substrate.
- 1 4. The package of claim 3, wherein the substrate and superstrate are formed of
- 2 material comprising PTFE with a ceramic filler.
- 1 5. The package of claim 1, wherein the plurality of layers includes at least 5 layers.
- 1 6. The package of claim 1, wherein a top one of the plurality of layers is sufficiently
- 2 rigid to maintain planarity of the package.
- 1 7. The package of claim 6, wherein the top layer is formed of FR4 epoxy glass
- 2 laminate.

1 8. The package of claim 1, wherein the bottom layer is formed of a glass reinforced
2 hydrocarbon/ceramic laminate.

1 9. The package of claim 8, wherein a layer formed below the substrate comprises a
2 glass reinforced hydrocarbon/ceramic laminate having an opening sized and shaped to
3 accommodate a chip carrier on which the integrated circuit is mounted.

1 10. The package of claim 1, wherein the contacts of the substrate are arranged to
2 accommodate a flip-chip mounting of the integrated circuit.

1 11. An integrated circuit package assembly, comprising:
2 an integrated circuit; and
3 a plurality of layers sealably connectable to each other to form a package having a
4 cavity sized and shaped to receive the integrated circuit, each layer being formed of a
5 respective material, each respective material being suitable for use as a printed circuit
6 board substrate,

7 at least one of the plurality of layers being a substrate having contacts that are
8 connectable to electrical contacts of the integrated circuit, and

9 a bottom one of the layers having a plurality of ball attach pads, electrically
10 connected to the contacts of the substrate.

1 12. The package assembly of claim 11, wherein one of the layers is a superstrate
2 above the substrate, the superstrate having a sufficiently high dielectric constant to
3 provide isolation between a plurality of signal traces on the substrate.

1 13. The package assembly of claim 12, wherein the superstrate is formed of the same
2 material as the substrate.

1 14. The package assembly of claim 13, wherein the substrate and superstrate are
2 formed of material comprising PTFE with a ceramic filler.

1 15. The package assembly of claim 11, wherein a top one of the plurality of layers is
2 formed of FR4 epoxy glass laminate.

1 16. The package assembly of claim 11, wherein the bottom layer is formed of a glass
2 reinforced hydrocarbon/ceramic laminate.

1 17. A printed circuit board assembly, comprising:

2 a printed circuit board having a circuit board substrate with circuit traces and a
3 plurality of devices thereon, said plurality of devices including at least one integrated
4 circuit package assembly that includes:

5 an integrated circuit; and

6 a plurality of layers sealably connectable to each other to form a package
7 having a cavity sized and shaped to receive the integrated circuit, each layer being
8 formed of a respective material, each respective material being of a type suitable
9 for use in the circuit board substrate,

10 at least one of the plurality of layers being a package substrate having
11 contacts that are connectable to electrical contacts of the integrated circuit, and

12 a bottom one of the layers having a plurality of ball attach pads,
13 electrically connected to contacts of the circuit board substrate.

1 18. The printed circuit board assembly of claim 17, wherein at least one of the
2 plurality of layers is formed from the same material as the printed circuit board substrate.

1 19. A method of making a package for an integrated circuit, comprising the steps of:

2 (a) providing a plurality of layers, each formed of a respective material suitable for
3 use as a printed circuit board substrate, at least one of the plurality of layers being a
4 substrate having contacts that are connectable to electrical contacts of the integrated
5 circuit, and

6 (b) sealably connecting the plurality of layers to each other to form a package having
7 a cavity sized and shaped to receive the integrated circuit, wherein a bottom one of the
8 layers has a plurality of ball attach pads that are electrically connected to the contacts of
9 the substrate.

- 1 20. The method of claim 19, wherein step (a) includes providing a superstrate above
- 2 the substrate, the superstrate having a sufficiently high dielectric constant to provide
- 3 isolation between a plurality of signal traces on the substrate.

- 1 21. The method of claim 20, wherein the superstrate is formed of the same material as
- 2 the substrate.

- 1 22. The method of claim 21, wherein the substrate and superstrate are formed of
- 2 material comprising PTFE with a ceramic filler.

- 1 23. The method of claim 19, wherein the plurality of layers includes at least 5 layers.

- 1 24. The method of claim 19, wherein a top one of the plurality of layers is sufficiently
- 2 rigid to maintain planarity of the package.

- 1 25. The method of claim 24, wherein the top layer is formed of FR4 epoxy glass
- 2 laminate.

- 1 26. The method of claim 19, wherein the bottom layer is formed of a glass reinforced
- 2 hydrocarbon/ceramic laminate.

- 1 27. The method of claim 26, wherein a layer formed below the substrate comprises a
- 2 glass reinforced hydrocarbon/ceramic laminate having an opening sized and shaped to
- 3 accommodate a chip carrier on which the integrated circuit is mounted.

- 1 28. The method of claim 19, wherein the contacts of the substrate are arranged to
- 2 accommodate a flip-chip mounting of the integrated circuit.